EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Philip S. Lyren (Reg. No. 40,709) on 9/3/09.

In the claims:

Rewrite the claims as follows:

a. Claim 1;

A distributed multiprocessing computer system, which includes a plurality of processors, each coupled to an associated memory module, wherein each of the associated memory modules stores data that is shared between said processors, said system comprising:

a Home processor that includes a memory block and a directory for said memory block in the associated memory module;

an Owner processor that includes a cache memory, and wherein said Owner processor obtains an exclusive copy of said memory block, and stores said exclusive copy of said memory block in said cache memory;

wherein said Owner processor begins write operations on said memory block and then displaces the exclusive copy of said memory block from said cache memory

prior to completing the write operations on said memory block, and in response to displacing said memory block prior to completing the write operations said Owner processor returns said displaced copy of said memory block to said Home processor with a signal indicating that said Owner processor remains a sharer of said memory block; and

wherein said Owner processor includes a register in which an address is stored representing a memory block obtained in response to a lock instruction, compares an address of any displaced data with the address stored in said register, and asserts a shared message if the address of any displaced data matches the address stored in said register.

b. Claim 4;

The distributed multiprocessing computer system of claim 1, wherein said lock instruction is a Load Lock instruction and said shared message is a Victim To Shared message

c. Claims 5 and 6 (Cancelled)

d. Claim 13;

A method of maintaining memory coherence in a distributed shared memory computer system including a plurality of processors, comprising:

requesting a copy of a memory block from a Home processor to perform a write operation on the copy of the memory block;

storing said copy of said memory block exclusively in a cache memory associated with an Owner processor;

updating a coherence directory for said memory block in said Home processor to indicate the write operation on the copy of said memory block in said cache memory associated with the Owner processor;

displacing said copy of said memory block from said cache memory prior to completion of said write operation on said memory block;

in response to commencing but not completing said write operation, transmitting a message from said Owner processor to said Home processor relinquishing exclusive control of said memory block, said message indicating that said Owner processor should still be deemed a sharer of said memory block and

wherein the copy of the memory block is requested using a Load Lock instruction from the Owner processor to the Home processor and transmitting a message includes assertion of a Victim To Shared message if an address of the displaced memory block matches an address of any memory block for which an exclusive copy resides in the Owner processor.

e. Claim 14 (Canceled)

f. Claim 18;

The method of claim 13, wherein the coherency directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message.

g. Claim 21;

A method of maintaining memory coherence in a distributed shared memory computer system including a plurality of processors, comprising:

requesting a copy of a memory block from a Home processor to perform write operations on the copy of the memory block;

storing said copy of said memory block exclusively in a cache memory associated with an Owner processor;

updating a coherence directory for said memory block in said Home processor to indicate the write operation on the copy of said memory block in said cache memory associated with the Owner processor;

displacing said copy of said memory block from said cache memory prior to completion of the write operations on said memory block;

in response to commencing but not completing said write operations, transmitting a message from said Owner processor to said Home processor relinquishing exclusive control of said memory block said message indicating that said Owner processor should still be deemed a sharer of said memory block;

asserting a request to again obtain an exclusive copy of said memory block, wherein, in response to the request to again obtain an exclusive copy of the memory block the Home processor determines if the Owner processor is a sharer of the memory block and if so, the Home processor sends an exclusive copy of the memory block to the Owner processor; and

wherein the copy of the memory block is requested using a lock instruction from the Owner processor to the Home processor and the Owner process transmits a share message if an address of the displaced memory block matches an address of any memory block for which an exclusive copy resides in the Owner processor.

h. 24.

A distributed multiprocessing computer system, comprising:

a first processor that includes a memory block and a directory associated with said memory block that tracks a status of said memory block;

a second processor that includes a cache memory, and wherein said second processor requests an exclusive copy of said memory block and stores said memory block in said cache memory;

wherein said second processor begins processing of said memory block and then displaces the exclusive copy of said memory block prior to completing the processing of said memory block, and in response to displacing said memory block but not completing the processing said second processor transmits a signal to said first processor indicating that said second processor relinquishes exclusive control of said memory block but should remain a sharer of said memory block; and

wherein said second processor includes a register in which an address is stored representing a memory block obtained in response to a lock instruction, compares an address of any displaced data with the address stored in said register, and asserts a shared message if the address of any displaced data matches the address stored in said register.

i. Claim 28;

The distributed multiprocessing computer system of claim 24, wherein the shared message is a Victim To Shared message.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHARLES E. ANYA whose telephone number is (571)272-3757. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Hyung S. Sough/
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09/14/09

cea.